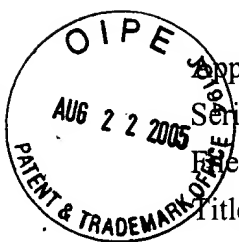


S/N 09/675,067

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant:	Samson X. Huang	Examiner:	Fritz Alphonse
Serial No.:	09/675,067	Group Art Unit:	2133
Filed:	September 28, 2000	Docket:	884.326US1
Title:	REPAIRABLE MEMORY IN DISPLAY DEVICES		
Assignee:	Intel Corporation	Customer Number:	21186

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The applicant requests review of the final rejection dated 18 April 2005 in the above-identified application. The applicant respectfully traverses all rejections. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated below:

I. Claims 1-6, 9-15, 20, 32-34, 38-39, and 41-43 were rejected under 35 USC § 103(a) as being unpatentable over Nishikawa in view of Shichiku.

The MPEP requires that a suggestion and a reasonable expectation of success be provided for a rejection based upon multiple references under 35 USC § 103. The suggestion to combine references and the reasonable expectation of success must both be found in the prior art.¹ The MPEP refers to "the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references."²

Nishikawa relates to an apparatus for reading and writing data including a rearranging circuit that rearranges bits of data having different significances when a region of a memory circuit has a defective portion. The final Office Action states that "Nishikawa does not explicitly discard the least significant bit... respective bits are rearranged so that the LSC is stored in the defect region."³

Shichiku relates to an image operation processing apparatus storing discrete data.⁴

¹ MPEP 2143.

² MPEP 2143.01.

³ Final Office Action, page 2.

⁴ Shichiku, Title.

Shichiku describes a method of storing data where “least significant bits are discarded.”⁵ The purpose of this method is to store data densely at continuous addresses instead of discretely. This method uses memory efficiently.⁶ The final Office Action improperly combines Nishikawa and Shichiku according to the following reason:

“it would have been obvious to improve upon the image operation processing apparatus, as disclosed by Shichiku. By doing so, it is possible to store data of the results of operation in continuous address of the memory, enabling efficient use of the memory areas.”⁷

The final Office Action has not shown evidence of a reasonable expectation of success of this combination. Nishikawa stores the LSB in a memory defect region.⁸ Nishikawa is storing data bits in a memory with defect regions. Shichiku discards least significant bits to store data densely at continuous addresses. If this method is used in Nishikawa, then important data will be stored in the defect regions of the memory used in Nishikawa. The data that Shichiku is storing will be corrupted by having some bits stored in defect regions. The final Office Action has not presented evidence that this combination of Nishikawa and Shichiku has a reasonable expectation of success. Specifically, the final Office Action has not shown evidence that the method of Shichiku can be implemented successfully with data corrupted by the defect regions in the memory of Nishikawa.

II. Claims 7-8, 16-19, 21-23, 35-37, and 40 were rejected under 35 USC § 103(a) as being unpatentable over Nishikawa, Shichiku, and Kondo (U.S. 5,153,574).

Kondo relates to an interface for a thin display panel having a timing circuit.⁹ Kondo describes the use of timing signals, and shows RAM memories with control circuits used to store color data. The final Office Action does not assert that Kondo provides a reasonable expectation of success of a combination of Nishikawa and Shichiku that is missing in the final Office Action. Therefore, the final Office Action has not shown that Nishikawa, Shichiku, and Kondo together support a *prima facie* case of obviousness of claims 1-6, 9-15, 20, 32-34, 38-39, and 41-43.

The final Office Action also does not identify a sufficient suggestion for combining

⁵ Shichiku, Col. 9, line 51.

⁶ Shichiku, Col. 9, line 57 to Col. 10, line 4.

⁷ Final Office Action, page 3.

⁸ Nishikawa, Col. 6, lines 4-16.

⁹ Kondo, Abstract.

Nishikawa and Shichiku with Kondo. The final Office Action states the following:

“It would have been obvious to use the memory defect routing of Nishikawa in a LCD display system with three memories for color display. This would have been obvious as suggested by Nishikawa wherein Nishikawa’s device is used for image data, “A rearranging circuit 12 has a function to rearrange respective bits representing image data...” col. 5, and lines 40-41 of Nishikawa.”¹⁰

Although both Kondo and Nishikawa may store image data in memory devices, this is completely irrelevant to the technical combination proposed in the final Office Action, which involves memory defect routing. The end use that stored data is put to (an image in the instant case) has no bearing on how that data is stored in a memory device, and the method of storing the data does not affect the resulting image.

No suggestion or motivation for combining Kondo with Nishikawa and Shichiku can be found in the references themselves. Kondo does not describe the inner-workings of the RAM memories, and in particular does not describe how the RAM memories compensate for defective cells. RAM memories are commercially available, and the inner-workings of such a RAM memory does not need to be known for Kondo to have a complete description. The RAM memories in Kondo are “black boxes” with inputs and outputs. Although Nishikawa has stated that its methods can be used with a RAM memory, the final Office Action has not provided evidence that the inner-workings of the RAM memory shown in Kondo could be operated according to the method of Nishikawa. The final Office Action has not provided evidence that the RAM memory shown in Kondo does or does not have a method to compensate for defective cells. Therefore, there is no evidence of a suggestion for the technical combination set forth in the final Office Action. Given that Kondo does not discuss the inner-workings of the RAM memory devices, the final Office Action has also not shown evidence of a reasonable expectation of success of applying the method of Nishikawa to manage defective cells in the RAM memory devices of Kondo.

The final Office Action states a rationale for combining Nishikawa, Shichiku and Kondo that is quoted in the applicant’s most recent response.¹¹ The final Office Action did not cite any evidence in Nishikawa, Shichiku or Kondo or any other prior art supporting the statements in the quoted paragraphs as is required by MPEP 2143. The final Office Action has not established a

¹⁰ Final Office Action, page 5.

¹¹ Final Office Action, page 5-6, quoted in applicant’s response filed 12 November 2004, pages 14-15.

motivation to combine Nishikawa and Shichiku with Kondo, or a reasonable expectation of success, based on these statements. The Examiner offered to provide references. A *prima facie* case of obviousness has not been established with the applied references Nishikawa, Shichiku, and Kondo. A simple addition of more references will not support a *prima facie* case of obviousness without evidence of a suggestion for the combination of these references and evidence of a reasonable expectation of success.


The applicant respectfully submits that a *prima facie* case of obviousness of claims 1-23 and 32-43 has not been established in the final Office Action, and that claims 1-23 and 32-43 are in condition for allowance. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

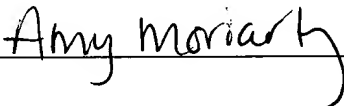
SAMSON X. HUANG

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938, Minneapolis, Minnesota 55402
(612) 373-6973

Date 18 AUGUST 2005 By 
Robert E Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18th day of August, 2005.

Name 

Signature 